**Lab 2**

**Power Management IC (PMIC)**

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**ECE 428/593B-001**

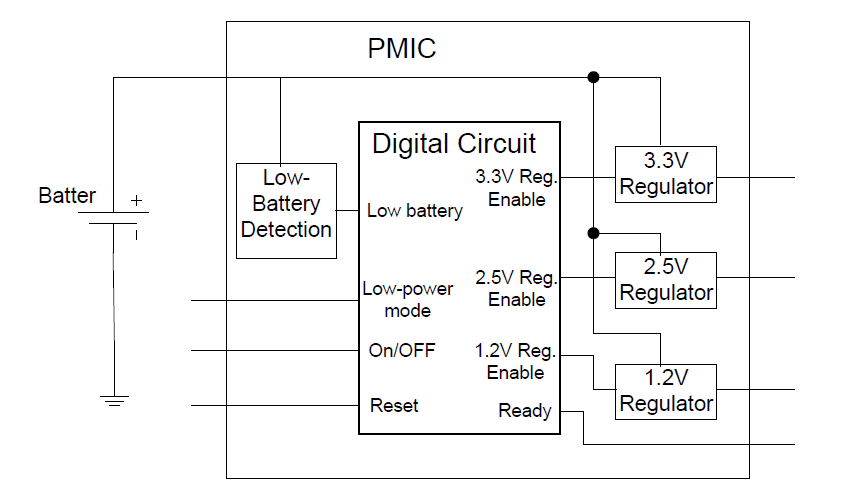
**Programmable ASIC Design**

**March 19, 2015**

# Specification

In this lab, students designed and constructed the digital portion of a power management integrated circuit (PMIC). The full integrated circuit accepts a high voltage as well as several inputs and provides several regulated voltages based on the value and timing of the inputs; the digital part of the circuit examines the value and timing of the inputs in order to control the regulators. A high-level diagram of the PMIC is provided in Figure 1.

Figure : High-Level Diagram of PMIC



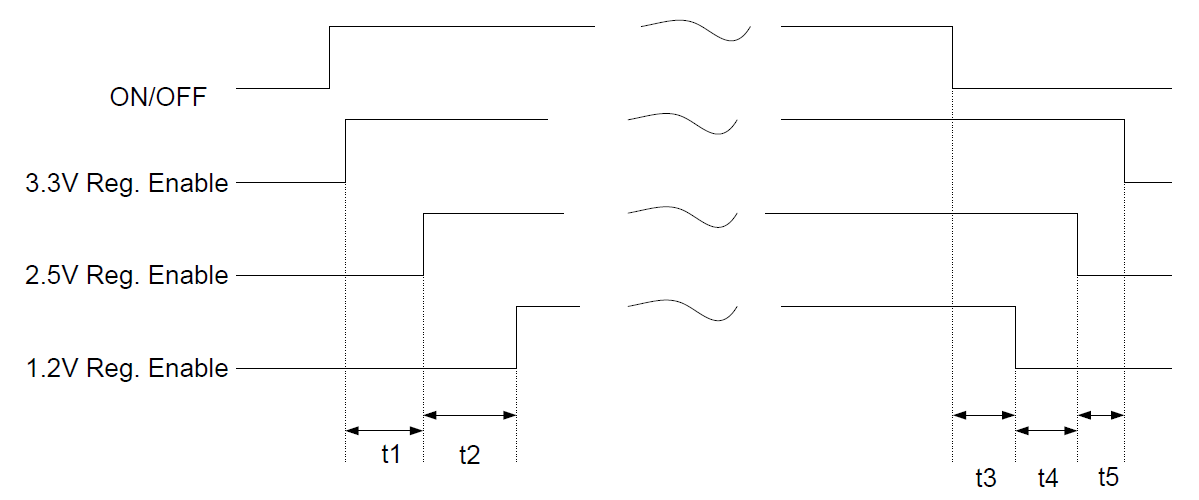
The digital part of the circuit accepts four input signals which include:

1. On/Off: When asserted, the PMIC begins booting up into full power mode or low power mode based on the value of the Low Power Mode signal as long as the Low Battery Detection signal is not asserted.
2. Low-Power Mode: When asserted while the On/Off signal is asserted, the PMIC begins booting up into low power mode; when not asserted while the On/Off signal is asserted, the PMIC begins booting up into full power mode.
3. Low-Battery Detection: When asserted while the On/Off signal is asserted, the PMIC automatically begins turning off; the PMIC will then remain off regardless of the other inputs until unasserted.
4. Reset: When asserted, the PMIC resets.

The digital part also provides four outputs which include the 3.3 V enable signal, 2.5 V enable signal, and 1.2 V enable signal which define when the appropriate regulators should be turned on and a ready signal which defines when the PMIC is not in the process of turning on or off regulators.

The process of enabling each regulator is dependent on both the combination of inputs that are asserted as well as a timing sequence. The process of booting up into full power mode is defined in Figure 2 where T1 = 1s, T2 = 1.5s, T3 = 1s, T4 = 0.5s, and T5 = 0.5s. The processes for booting up into low power mode and for transitioning to low power mode from full power mode and to full power mode from low power mode should be defined as part of the design.

Figure : Process for Booting Up into Full Power Mode



# Design

## Coarse Enumeration of States and State Transitions

The design must provide routines to boot from no power to full power, from full power to no power, from no power to low power, from low power to no power, from low power to full power, and from full power to low power; additionally, the full power and low power states must have the capability of shutting down when a low battery is sensed, and the no power state must have the capability of staying shut down when a low battery is sensed. From this, it can be seen that there must be three terminal states: (1) the off state, (2) the full power or on state, and (3) the low power state. It is assumed that any transition between terminal states is allowed to complete before another transition between terminal states is started; this reduces design complexity by eliminating many edges in the finite state machine.

## Definition of Timing for State Transitions

The full power-up and full power-down routines are strongly defined by the requirements; it is stated that each routine should follow the timing diagram shown in Figure 2. Table 1 tabulates the delay of each action in the routine with respect to the action that starts the routine.

Table : Timing for Full Power-Up and Power-Down Routines

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Full Power Up** | | | **Full Power Down** | | |
| *Measured from Power On Time* | | | *Measured from Power Off Time* | | |
| **State** | **Delay** | **Derivation** | **State** | **Delay** | **Derivation** |
| 3.3 V Enable | 0 s | T0 | 1.2 V Disable | 1.0 s | T3 |
| 2.5 V Enable | 1.0 s | T0 + T1 | 2.5 V Disable | 1.5 s | T3 + T4 |
| 1.2 V Enable | 2.5 s | T0 + T1 + T2 | 3.3 V Disable | 2.0 s | T3 + T4 + T5 |

The low power-up and low power-down routines are weakly defined by the requirements; it is suggested that each routine should follow the timing diagram shown in Figure 2, but it is never stated which part of the timing diagram should be used. For the given design, it has been adopted from the timing diagram that the first step in each start-up routine should be done with T0 delay and the first step in each shut-down routine should be done with T3 delay. Table 2 tabulates the delay of each action in the routine with respect to the action that starts the routine.

Table : Timing for Low Power-Up and Power-Down Routines

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Low Power Up** | | | **Low Power Down** | | |
| *Measured from Power On Time* | | | *Measured from Power Off Time* | | |
| **State** | **Delay** | **Derivation** | **State** | **Delay** | **Derivation** |
| 1.2 V Enable | 0 s | T0 | 1.2 V Disable | 1.0 s | T3 |

The transitions from full power to low power and from low power to full power are not defined by the requirements. The standard described for the low power-up and low power-down routines has been adopted so that the first step in the low power to full power routine should be done with T0 delay and the first step in the full power to low power routine should be done with T3 delay; additionally, it has been adopted that the second step in the low power to full power routine should be done with T1 delay and the second step in the full power to low power routine should be done with T4 delay. This decision creates symmetry between all the start-up and shut-down routines that leads to predictable system operation. Table 3 tabulates the delay of each action in the routine with respect to the action that starts the routine.

Table : Timing for Full-to-Low Power and Low-to-Full Power Transitions

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Full Power to Low Power** | | | **Low Power to Full Power** | | |
| *Measured from Power On Time* | | | *Measured from Power Off Time* | | |
| **State** | **Delay** | **Derivation** | **State** | **Delay** | **Derivation** |
| 2.5 V Disable | 1.0 s | T3 | 3.3 V Enable | 0 s | T0 |
| 3.3 V Disable | 1.5 s | T3 + T4 | 2.5 V Enable | 1.0 s | T0 + T1 |

## Detailed Enumeration of States

Given the coarse enumeration and definition of timing for both the states and state transitions, it is possible to provide a detailed enumeration of the states and description of state transitions. An enumeration of all the states is provided in Table 1; a state transition diagram relating the states with the state transitions is provided at the conclusion of this report.

## Enumeration of Components

Given the design described so far, it is simple to identify the various components that will be needed in the design:

1. The operation of the power management integrated circuit has been described in terms of states and state transitions; this description can be implemented using a finite state machines.
2. The state transitions must occur after a certain delay; this delay can be measured using a timer implemented using a counter and a comparator.
3. The finite state machine and the timer should be synchronized by a clock with a period and skew that is well controlled; this clock can be implemented using a digital clock manager.

These three components—a finite state machine, a timer, and a digital clock manager—will represent sub-modules under the power management integrated circuit module.

Table : Enumeration of States in Finite State Machine

|  |  |
| --- | --- |
| **State** | **Description** |
| Off | No power is being supplied. The circuit may start a transition into full power (after 0s delay) or low power (after 0s delay) if the battery is not low. |
| On | Full power is being supplied on the 1.2 V, 2.5 V, and 3.3 V rails. The circuit may start a transition into no power (after 1s delay) or low power (after 1s delay); if the battery is low, the circuit must automatically start a transition into no power. |
| Low Power | Low power is being supplied on the 1.2 V rail only. The circuit may start a transition into no power (after 1s delay) or full power (after 0s delay); if the battery is low, the circuit must automatically start a transition into no power. |
| Low Battery | The battery is determined to be low while the circuit is in the On state. The circuit must automatically start a transition into no power. |
| Low Battery in Low Power | The battery is determined to be low while the circuit is in the Low Power state. The circuit must automatically start a transition into no power. |
| 3.3 V Enable | The 3.3 V rail is enabled. The circuit may transition into the 2.5 V Enable state (after 1s delay). |
| 2.5 V Enable | The 3.3 V and 2.5 V rails are enabled. The circuit may transition into the 1.2 V Enable state (after 1.5s delay). |
| 1.2 V Enable | The 3.3 V, 2.5 V, and 1.2 V rails are enabled. The circuit may transition into the On state (after 0s delay). |
| 1.2 V Disable | The 3.3 V and 2.5 V rails are enabled. The circuit may transition into the 2.5 V Disable state (after 0.5s delay). |
| 2.5 V Disable | The 3.3 V rail is enabled. The circuit may transition into the 3.3 V Disable state (after 0.5s delay). |
| 3.3 V Disable | No rails are enabled. The circuit may transition into the Off state (after 0s delay). |
| 1.2 V Enable with Low Power | The 1.2 V rail is enabled. The circuit may transition into the Low Power state (after 0s delay). |
| 1.2 V Disable with Low Power | No rails are enabled. The circuit may transition into the Off state (after 0s delay). |
| 3.3 V Enable from Low Power | The 1.2 V and 3.3 V rails are enabled. The circuit may transition into the 2.5 V Enable from Low Power state (after 1s delay). |
| 2.5 V Enable from Low Power | The 1.2 V, 3.3 V, and 2.5 V rails are enabled. The circuit may transition into the On state (after 0s delay). |
| 2.5 V Disable into Low Power | The 1.2 V and 3.3 V rails are enabled. The circuit may transition into the 3.3 V Disable into Low Power state (after 0.5s delay). |
| 3.3 V Disable into Low Power | The 1.2 V rail is enabled. The circuit may transition into the Low Power state (after 0s delay). |

# Implementation

## Description of Timing

The Atlys Development Board provides a 100 MHz CMOS oscillator capable of providing a clock signal to the included FPGA. Since the timer needed to count upwards of one and a half seconds of clock pulses at this speed is large and since the speed is not actually needed for this application, the clock is divided by 10 to provide a 10 MHz clock signal to all components internal to the FPGA.

The design requires time divisions of 0.5 second, 1 second, and 1.5 seconds to properly operate which correspond to 5 million, 10 million, and 15 million clock pulses under a 10 MHz clock signal. The time divisions along with the number of clock cycles and associated symbols are given in Table 5; each line in the table represents an input to the timer sub-module that is used in a comparison against the current value of the timer.

Table : Definition of Time Periods with Number of Clock Cycles

|  |  |  |
| --- | --- | --- |
| **Symbol** | **Time Period** | **Number of Clock Cycles** |
| T1 | 1s | 10,000,000 |
| T2 | 1.5s | 15,000,000 |
| T3 | 1s | 10,000,000 |
| T4 | 0.5s | 5,000,000 |
| T5 | 0.5s | 5,000,000 |

## Description of Modules and Sub-Modules

The power management integrated circuit consists of three modules: a timer module, a finite state machine module, and a digital clock management module.

The timer module was written in VHDL using a behavioral style. It consists of a counter sub-module and a set of five comparator sub-modules; it accepts as input a clock signal and a reset signal, and it takes as parameter five integers. On every clock edge, the counter is incremented by one and is compared against the five integers; when the counter is greater than or equal to one of the five integers, an output is asserted. In this way, the timer module is capable of timing up to five events that all start at one time.

The finite state machine module was written in VHDL using a behavioral style. It accepts as input five timer signals, an on/off signal, a low battery signal, a low power signal, a clock signal, and a reset signal; it provides as output a 3.3 V enable signal, a 2.5 V enable signal, a 1.2 V enable signal, a ready signal, and a timer reset signal. Each state in the finite state machine represents a combination of voltages that are currently being used by the power management integrated circuit; each transition in the finite state machine implements different functions (i.e. full power, low power, or low battery shutdown).

The digital clock management module was implemented using the IP Core Generator in the Xilinx ISE Design Suite. It is used for two purposes: (1) to control skew on the clock and (2) to divide the 100 MHz signal provided by the oscillator on the development board into a 10 MHz signal used by the circuit on the FPGA.

The three modules have been implemented together in a top-level module implemented in VHDL using a structural style. The timer reset output of the finite state machine module is used as a reset input to the timer module. The outputs of the timer module are used as inputs to the finite state machine module. The output of the digital clock management module is used to drive both the timer module and the finite state machine module. All other inputs are tied to the finite state machine module. In this way, the finite state machine can determine which voltages are being used at any given time and can provided timed transitions when different voltages are needed.

## Mapping of Signals to Development Board

The inputs to the power management integrated circuit consist of the on/off signal, the low power signal, the low battery signal, the clock signal, and the reset signal. The on/off signal, the low power signal, and the low battery signal are mapped to slide switches on pins A10, D14, and C14, respectively. The clock signal is mapped to the oscillator on pin L15. The reset signal is mapped to a push button on pin N4.

The outputs from the integrated circuit consist of the 1.2 V enable signal, the 2.5 V enable signal, the 3.3 V enable signal, and the ready signal which are mapped to pins U18, M14, N14, and L14, respectively.

# Simulation

To ensure proper operation of the design, a testbench was written in VHDL that tests each of the major transitions through the finite state machine. The testbench consists of six tests: (1) start up into and shut down from full power, (2) start up into and shut down from low power, (3) transition from low power and full power, (4) start up with low battery, (5) shut down from full power with low battery, and (6) shut down from low power with low battery.

A 100 MHz clock was provided to the testbench to replicate the 100 MHz oscillator provided by the development board. To reduce simulation time, the time divisions used by the timer were reduced by three orders of magnitude; this preserves the functionality of the circuit while compressing all operations from the range of seconds to the range of milliseconds.

Proper operation of the design can be verified by checking the waveforms generated by the testbench against the specifications provided in both the Specification section and the Design section. The waveforms corresponding to a behavioral simulation of the testbench are included at the conclusion of this report; careful analysis will reveal that these waveforms do indeed meet specifications.

# Conclusion

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