**Lab 2**

**Power Management IC (PMIC)**

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**Prepared for:**

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**ECE 428/593B-001**

**Programmable ASIC Design**

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# Purpose

The purpose of this lab is to

# Procedure

In

1. In the

Following the procedure, it is suggested that students examine the schematic and timing facilities provided after the synthesis and implementation steps in the design flow.

# Discussion

## High-Level Design

The

## High-Level Verification

The VHDL

## Simulation

To

## Synthesized Schematic

After

## Implemented Schematic

After

## Static Timing Analysis

A

# Extension: Modifying Pin Assignments

## Purpose

In

## Procedure

The procedure is largely the same as for the main part of the lab except that the following change is made:

1. Modify

## Results

After

# References

|  |  |
| --- | --- |
| [1] | Digilent, Inc., "Atlys Board Reference Manual," 2 May 2013. [Online]. Available: http://www.digilentinc.com/Data/Products/ATLYS/Atlys\_rm\_V2.pdf. [Accessed 18 February 2015]. |